EE/CprE/SE 491 WEEKLY REPORT 9

Date: ***Apr 10th, 2023 – Apr 16th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Weekly Summary

During this past week, we made more progress toward understanding how ReRAM works in the Skywater 130 nm process. There are still some lingering questions about how the "forming" is done and how often it is done. But we have a good understanding now of how setting and resetting the cells work. Outside of that, we also made more progress toward getting a simulation of the ReRAM cell. We still have not successfully simulated it, but we are very close, as we just have to tweak some software. We also made more progress on building some of our components and creating layouts of them as well.

Past week accomplishments

- Joshua Thater
    - Researched more into how ReRAM works in the Skywater 130 nm process
        - Figured out how "setting" and "resetting" is done for the ReRAM cells
        - Developed a good understanding of how we will write weights to ReRAM cells through this setting and resetting
        - Link to documentation: https://sky130-fd-pr-reram.readthedocs.io/en/latest/
    - Began the process of simulating the ReRAM device
        - Download Trilinos, ADMS, & Xyce
            - Configured Xyce incorrectly, so have to rebuild it and try again

- Aiden Petersen
    - Research into ReRAM
        - Understanding setting and resetting
        - Understand forming process
    - Created a new top level diagram of the project with more detailed features and updated knowledge on setting and resetting.
- Matt Ottersen
    - Worked on getting the Op Amp to pass LVS
- Regassa Dukele
    - Re-designed ADC and did a simulation
    - Worked on simulation errors that ADC processed

Pending issues

- How to configure Xyce to properly convert Verilog-A netlist to Xyce readable netlist
- How to properly create a layout of ReRAM cell using Magic
- Issues with figuring out how metal layers work and interconnect with vias in Magic

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Researched more into ReRAM, and attempted to simulate ReRAM cell through Xyce	5	57
Aiden Petersen	ReRAM research, toplevel schematic.	5	45
Matt Ottersen	○ Worked on getting the Op Amp to pass LVS	4	48
Regassa Dukele	Re-designed ADC and did a simulation	5	48.5

Plans for the upcoming week

- Joshua Thater
    - Rebuild Xyce with the proper configurations
    - Convert Verilog-A netlist of ReRAM into Xyce readable netlist and simulate
    - Try to simulate other components with Xyce if time allows
- Aiden Petersen
    - Continue ReRAM research, may start xyce sims
- Matt Ottersen
    - Get Op Amp to Pass LVS
    - Create a layout by using other manually made layouts (1bit ADC from OpAmp)

- Regassa Dukele
    - Make ADC layout and do more research on its integration